Exhibit 34

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571–272–7822

Paper 14
Entered: March 11, 2015

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

EMC CORPORATION,
Petitioner,

v.

ACQIS LLC,
Patent Owner.

Case IPR2014-01462
Patent 8,041,873 B2

Before MICHAEL P. TIERNEY, MICHAEL J. FITZPATRICK, and ROBERT J. WEINSCHENK, *Administrative Patent Judges*.

WEINSCHENK, *Administrative Patent Judge*.

DECISION
Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

EMC Corporation ("Petitioner") filed a Petition[1] (Paper 2; "Pet." or "Petition") requesting *inter partes* review of claims 54 and 56–61 of U.S. Patent No. 8,041,873 B2 (Ex. 1001; "the '873 patent"). ACQIS LLC ("Patent Owner") filed a Preliminary Response to the Petition. Paper 11 ("Prelim. Resp."). We have jurisdiction under 35 U.S.C. § 314, which provides that an *inter partes* review may not be instituted "unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a).

For the reasons set forth below, on this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing the unpatentability of claims 54 and 56–61 of the '873 patent. Accordingly, we institute *inter partes* review as to claims 54 and 56–61 of the '873 patent on the grounds specified below.

A. *Related Proceedings*

The parties indicate that the '873 patent is at issue in the following district court cases: *ACQIS LLC v. Alcatel-Lucent USA, Inc.*, No. 6:13-cv-00638 (E.D. Tex.); *ACQIS LLC v. EMC Corp.*, No. 6:13-cv-00639 (E.D. Tex.); *ACQIS LLC v. Ericsson, Inc.*, No. 6:13-cv-00640 (E.D. Tex.); and *ACQIS LLC v. Huawei Technologies Co.*, No. 6:13-cv-00641 (E.D. Tex.). Pet. 56–57; Paper 8, 2.

Petitioner identifies the following *inter partes* review proceedings as being related to this proceeding (Pet. 57):

[1] Petitioner filed a corrected petition (Paper 4) without a motion or authorization. *See* 37 C.F.R. § 42.104(c). For purposes of this decision, we rely on the first filed petition.

IPR Case No.	Involved U.S. Patent No.
IPR2014-01452	RE43,171 E
IPR2014-01469	RE42,814 E

B. *The '873 Patent*

The '873 patent relates to interfacing two Peripheral Component Interconnect ("PCI") buses using a non-PCI channel. Ex. 1001, col. 5, ll. 31–33, Fig. 6. More specifically, PCI address and data bits are encoded and then converted from a parallel format to a serial format. *Id.* at col. 16, ll. 55–58, Fig. 10. The information is transmitted in a serial format over a non-PCI channel, and, when received, the information is converted back into a parallel format and decoded so it is suitable for transmission on a PCI bus. *Id.* at col. 16, ll. 58–60, Fig. 11.

C. *Illustrative Claim*

Claim 54 is independent and is reproduced below.

> 54. A computer module insertable into a coupling site of a console for data communication, comprising:
>
> a main circuit board;
>
> a processing unit coupled to the main circuit board;
>
> a main memory coupled to the processing unit;
>
> a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction; and
>
> a peripheral bridge directly coupled to the processing unit, the peripheral bridge comprising an interface controller directly coupled to the LVDS channel.

Id. at col. 43, ll. 40–52.

D. *References*

Petitioner relies on the following references and declaration (*see* Pet. 58–59):

Reference or Declaration	Exhibit No.
U.S. Patent No. 5,608,608 ("Flint")	Ex. 1002
Declaration of Bruce Young[2]	Ex. 1003
Robert W. Horst, TNet: A Reliable System Area Network ("Horst")	Ex. 1011
U.S. Patent No. 6,148,357 ("Gulick")	Ex. 1012
A. Bogaerts et al., RD24 Status Report: Application of the Scalable Coherent Interface to Data Acquisition at LHC ("Bogaerts")	Ex. 1013
U.S. Patent No. 5,428,806 ("Pocrass")	Ex. 1016
U.S. Patent No. 5,227,957 ("Deters")	Ex. 1017
U.S. Patent No. 5,961,623 ("James")	Ex. 1018
National Semiconductor, LVDS Owner's Manual: Design Guide ("LVDS Owner's Manual")	Ex. 1019

E. *Asserted Grounds of Unpatentability*

Petitioner asserts that the challenged claims are unpatentable on the following grounds[3] (*see* Pet. 58–60):

Claims Challenged	Basis	References
54 and 56–61	35 U.S.C. § 102(b)	Flint
54, 57, 60, and 61	35 U.S.C. § 102(b)	Horst
56 and 59	35 U.S.C. § 103(a)	Horst and Pocrass
58	35 U.S.C. § 103(a)	Horst and Deters

[2] Petitioner filed two corrected Declarations of Bruce Young (Papers 5, 6) without a motion or authorization. For purposes of this decision, we rely on the first filed Declaration.

[3] Patent Owner argues that the obviousness combinations are asserted in the alternative, and, thus, should be denied. Prelim. Resp. 23–32. The decisions cited by Patent Owner in support of that argument are not binding precedent and do not require that alternative combinations be denied, and we do not deny any grounds asserted in the Petition on that basis.

Claims Challenged	Basis	References
54, 57, 60, and 61	35 U.S.C. § 103(a)	Bogaerts and James or Gulick
56 and 59	35 U.S.C. § 103(a)	Bogaerts, Pocrass, and James or Gulick
58	35 U.S.C. § 103(a)	Bogaerts, Deters, and James or Gulick
54 and 56–61	35 U.S.C. § 103(a)	Any of the grounds above and LVDS Owner's Manual

II. ANALYSIS

A. *Claim Construction*

The claims of an unexpired patent are interpreted using the broadest reasonable interpretation in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012). On this record and for purposes of this decision, the only claim terms requiring express construction are the terms "Peripheral Component Interconnect (PCI) bus transaction" and "PCI bus transaction."

Petitioner proposes construing the term "Peripheral Component Interconnect (PCI) bus transaction" in the challenged claims to mean "a data signal communication with an interconnected peripheral component." Pet. 14. Petitioner argues that its proposed construction is supported by a decision of the U.S. District Court for the Eastern District of Texas construing a similar term in related, but different, patents. *Id.* at 13–15. Patent Owner proposes construing the term "Peripheral Component Interconnect (PCI) bus transaction" in the challenged claims to mean "command, address, and data information, in accordance with the PCI standard, for communication with an interconnected peripheral component."

Prelim. Resp. 4. Patent Owner argues that its proposed construction is supported by the claim language, the specification of the '873 patent, and certain extrinsic evidence. *Id.* at 5–12. The dispute between the parties focuses on whether the term "Peripheral Component Interconnect (PCI)" refers to the PCI industry standard.

On this record and for purposes of this decision, we agree with Patent Owner that the term "Peripheral Component Interconnect (PCI)" refers to the PCI industry standard. Industry literature and dictionaries use the proper noun "Peripheral Component Interconnect" and the abbreviation "PCI" to refer to a particular industry specification for a local bus. *See, e.g.*, Ex. 2001, 1; Ex. 2002, 6–7; Ex. 2003, 7–8. The challenged claims also recite "Peripheral Component Interconnect" as a proper noun and abbreviate it as "PCI" (Ex. 1001, col. 43, ll. 48–49, col. 44, l. 6), indicating that the challenged claims use those terms consistent with the understood industry meaning. *See Azure Networks, LLC v. CSR PLC*, 771 F.3d 1336, 1348 (Fed. Cir. 2014). The specification of the '873 patent also supports Patent Owner's proposed construction. For example, the specification uses the common noun "peripheral bus" when referring generally to a peripheral bus. *See, e.g.*, Ex. 1001, col. 10, ll. 53–55 ("Additionally, the peripheral controller is coupled to a clock control logic, a configuration signal, and *a peripheral bus*.") (emphasis added). Thus, the challenged claims could have used the term "peripheral component bus transaction," but instead recite a "Peripheral Component Interconnect (PCI) bus transaction." Further, Petitioner's declarant in this proceeding, Mr. Bruce Young, admits that the term "Peripheral Component Interconnect (PCI)" refers to an industry

standard (Ex. 1003 ¶ 58), and Petitioner admits the same in the related district court case (Ex. 2006, 1, 3).

The only evidence Petitioner offers in support of its proposed construction is the claim construction order issued in *ACQIS LLC v. Appro International, Inc.*, No. 6:09-cv-00148 (E.D. Tex. Feb. 3, 2011). Pet. 13–15; Ex. 1015. In that case, the district court considered related, but different, patents. Pet. 13. Also, the parties in that case did not appear to dispute that the term "Peripheral Component Interconnect (PCI)" refers to an industry standard. Rather, the dispute before the district court focused on which particular bus architectures of the PCI industry standard were covered by the term "PCI bus transaction." Ex. 1015, 7 ("The parties' primary dispute is whether the term is limited to the conventional, parallel PCI Local Bus, and, therefore excludes PCI Express bus architecture and bus transaction protocol.").

Therefore, on this record and for purposes of this decision, the broadest reasonable interpretation of the claim terms "Peripheral Component Interconnect (PCI) bus transaction" and "PCI bus transaction" is "Peripheral Component Interconnect (PCI) industry standard bus transaction."

B. *Asserted Grounds of Unpatentability*

1. *Anticipation of Claims 54 and 56–61 by Flint*

Petitioner argues that claims 54 and 56–61 are anticipated by Flint. Pet. 59. Flint relates to a cartridge-based design for computers. Ex. 1002, col. 2, ll. 18–21. We have reviewed Petitioner's assertions and supporting evidence, and, for the reasons discussed below, Petitioner does *not* demonstrate a reasonable likelihood of prevailing in showing that Flint anticipates claims 54 and 56–61.

Each independent claim challenged by Petitioner recites an encoded serial bit stream of a Peripheral Component Interconnect (PCI) bus transaction. Ex. 1001, col. 43, ll. 48–49. Petitioner argues that Flint discloses this limitation because the local bus interface 218 communicates "with a number of peripheral components in the chassis and cartridge through the I/O interface, an expansion bus interface, and PCMCIA interfaces via the common bus (220, 300, 102)." Pet. 22–23. Petitioner does not argue that Flint discloses an encoded serial bit stream of a PCI industry standard bus transaction. *Id.* Petitioner's argument instead is premised on the claim term "Peripheral Component Interconnect (PCI) bus transaction" being construed to refer to a communication with any interconnected peripheral component. *Id.*; Prelim. Resp. 9. For the reasons discussed above, the claim term "Peripheral Component Interconnect (PCI) bus transaction" refers to the PCI industry standard. *See* Section II.A. Thus, on this record, Petitioner does *not* demonstrate a reasonable likelihood of prevailing in showing that Flint anticipates claims 54 and 56–61.

2. *Anticipation of Claims 54, 57, 60, and 61 by Horst*

Petitioner argues that claims 54, 57, 60, and 61 are anticipated by Horst. Pet. 59. Horst relates to a system area network called TNet that is designed for reliable, efficient communications among processors and peripherals. Ex. 1011, 1. We have reviewed Petitioner's assertions and supporting evidence, and, for the reasons discussed below, Petitioner does *not* demonstrate a reasonable likelihood of prevailing in showing that Horst anticipates claims 54, 57, 60, and 61.

Each independent claim challenged by Petitioner recites a low voltage differential signal (LVDS) channel. Ex. 1001, col. 43, l. 45. Petitioner

argues that "Horst teaches that TNet links include low voltage, differential ECL data links (*i.e.*, a LVDS channel)" and cites generally to pages 3 and 4 of Horst as support for that argument. Pet. 31. Horst discloses that "[i]ntercabinet links use differential emitter-coupled logic drivers to drive up to 20 meters of cable." Ex. 1011, 4. However, Petitioner does not identify with specificity anything in Horst that expressly discloses that the differential emitter-coupled logic drivers are *low voltage*, and Petitioner does not argue that Horst inherently discloses that the differential emitter-coupled logic drivers are *low voltage*. Pet. 31; Ex. 1003 ¶¶ 76, 127, 131[54D]. Petitioner instead admits that later implementations of the TNet system (not the one disclosed in Horst) use LVDS signaling. Pet. 31. Therefore, on this record, Petitioner does *not* demonstrate a reasonable likelihood of prevailing in showing that Horst anticipates claims 54, 57, 60, and 61.

3. *Obviousness of Claims 54, 57, 60 and 61 over Horst and LVDS Owner's Manual*

Petitioner argues that claims 54, 57, 60, and 61 would have been obvious over Horst and the LVDS Owner's Manual. Pet. 59–60. We have reviewed Petitioner's assertions and supporting evidence, and, for the reasons discussed below, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claims 54, 57, 60, and 61 would have been obvious over Horst and the LVDS Owner's Manual.

Independent claim 54 recites a computer module comprising "a main circuit board." Ex. 1001, col. 43, l. 42. Petitioner identifies the processor node in Horst as being the recited computer module. Pet. 29–30. Petitioner argues that the processor node in Horst includes a TNet processor interface application-specific integrated circuit ("ASIC"), and that a person of ordinary skill in the art would have understood that an ASIC was

implemented on a circuit board. Pet. 30; Ex. 1011, 6, Fig. 7; Ex. 1003 ¶ 127. On this record, Petitioner has shown sufficiently that Horst teaches the above limitation of claim 54.

Independent claim 54 recites "a processing unit coupled to the main circuit board." Ex. 1001, col. 43, l. 43. Petitioner argues that the processor node in Horst includes a CPU coupled to the TNet processor interface ASIC (Pet. 30; Ex. 1011, Fig. 7), which, as discussed above, would have been implemented on a circuit board. On this record, Petitioner has shown sufficiently that Horst teaches the above limitation of claim 54.

Independent claim 54 recites "a main memory coupled to the processing unit." Ex. 1001, col. 43, l. 44. Petitioner argues that the processor node in Horst includes a main memory coupled to the CPU through the TNet processor interface. Pet. 30; Ex. 1011, Fig. 7. On this record, Petitioner has shown sufficiently that Horst teaches the above limitation of claim 54.

Independent claim 54 recites "a low voltage differential signal (LVDS) channel comprising two sets of unidirectional, multiple serial bit channels to transmit data in opposite directions." Ex. 1001, col. 43, ll. 45–49. Petitioner argues that Horst teaches byte-serial data links with independent transmit and receive channels to transmit data in opposite directions. Pet. 31; Ex. 1011, 3, Fig. 3. Petitioner also argues that the byte-serial data links in Horst comprise differential emitter-coupled logic drivers. Pet. 31; Ex. 1011, 4, Fig. 4. However, as discussed above in Section II.B.2, Petitioner does not identify with specificity anything in Horst that teaches that the byte-serial data links are *low voltage*. Pet. 31; Ex. 1003 ¶¶ 76, 127, 131[54D]. Petitioner argues that the LVDS Owner's Manual teaches a low

voltage differential signal ("LVDS") channel. Pet. 50; Ex. 1019, 3. According to Petitioner, the LVDS Owner's Manual teaches that an LVDS channel can be used for peripheral links and rack-to-rack systems, and, thus, it would have been obvious to use the LVDS channel taught by the LVDS Owner's Manual for the peripheral links in the rack-to-rack system in Horst. Pet. 50–51; Ex. 1019, 8.

Patent Owner argues that Petitioner fails to explain how the teachings of the LVDS Owner's Manual would have been combined with Horst or provide a description of the resulting combination. Prelim. Resp. 45–46. Patent Owner's argument is not persuasive. As discussed above, Petitioner explains that Horst uses a differential signal channel, and that the LVDS Owner's Manual teaches a specific type of differential signal channel, namely an LVDS channel, that is suitable for systems like the one in Horst. Thus, on this record, Petitioner demonstrates that one of ordinary skill in the art would have had sufficient reason to use the LVDS channel taught by the LVDS Owner's Manual as the differential signal channel in the system taught by Horst.

Independent claim 54 recites that the LVDS channel is "for communicating an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction." Ex. 1001, col. 43, ll. 45–49. Petitioner argues that the TNet processor interface in Horst encodes the information transmitted on the byte-serial data links. Pet. 31–32; Ex. 1011, Fig. 4 ("8B/9B encoder"). Petitioner also argues that the byte-serial data links in Horst communicate with peripheral devices that use PCI industry standard buses. Pet. 31; Ex. 1011, 7 ("Different versions of the bus interface logic support industry standard buses such as VME and the peripheral component

interconnect (PCI).”). Patent Owner argues that Petitioner’s overly broad construction of the term “Peripheral Component Interconnect (PCI) bus transaction” is fatal to Petitioner’s reliance on Horst. Prelim. Resp. 9–10. Patent Owner does not address, however, the portion of Horst discussed above that expressly discloses communicating with peripheral devices that use PCI industry standard buses. On this record, Petitioner has shown sufficiently that the combination of Horst and the LVDS Owner’s Manual teaches the above limitation of claim 54.

Independent claim 54 recites “a peripheral bridge directly coupled to the processing unit, the peripheral bridge comprising an interface controller directly coupled to the LVDS channel.” Ex. 1001, col. 43, ll. 50–52. Petitioner argues that the TNet processor interface in Horst is a peripheral bridge that is directly coupled to the CPU and includes an interface controller that is directly coupled to the byte-serial data links. Pet. 32; Ex. 1011, Fig. 7. On this record, Petitioner has shown sufficiently that Horst teaches the above limitation of claim 54. Therefore, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 54 would have been obvious over Horst and the LVDS Owner’s Manual.

Dependent claim 57 depends from claim 54 and further recites that “the computer module is configured to operate upon receiving power from the console.” Ex. 1001, col. 43, ll. 58–60. Petitioner argues that Horst contemplates isolation and containment of power faults, which is only possible if power is provided to the computer module through the console. Pet. 32; Ex. 1003 ¶¶ 126, 131[57] . On this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 57 would have been obvious over Horst and the LVDS Owner’s Manual.

Dependent claim 60 depends from claim 54 and further recites that "the peripheral bridge corresponds to a north bridge." Ex. 1001, col. 44, ll. 3–4. Petitioner argues that the TNet processor interface in Horst corresponds to a north bridge. Pet. 33; Ex. 1011, Fig. 7. On this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 60 would have been obvious over Horst and the LVDS Owner's Manual.

Dependent claim 61 depends from claim 54 and further recites that "the encoded serial bit stream of PCI bus transaction comprises encoded PCI address and data bits." Ex. 1001, col. 44, ll. 5–7. Petitioner argues that, because the TNet system in Horst allows any CPU to communicate with any other CPU or I/O controller in the network, one of ordinary skill in the art would have understood that the bit stream included both address and data bits. Pet. 33; Ex. 1011, 1. On this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 61 would have been obvious over Horst and the LVDS Owner's Manual.

4. *Obviousness of Claims 56 and 59 over Horst, LVDS Owner's Manual, and Pocrass*

Petitioner argues that claims 56 and 59 would have been obvious over Horst, the LVDS Owner's Manual, and Pocrass. Pet. 59–60. We have reviewed Petitioner's assertions and supporting evidence, and, for the reasons discussed below, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claims 56 and 59 would have been obvious over Horst, the LVDS Owner's Manual, and Pocrass.

Claim 56 depends from claim 54 and further recites that the computer module comprises "a serial communication controller to couple to the console for data communication." Ex. 1001, col. 43, ll. 55–57. Petitioner

argues that the processor node in Horst includes a TNet processor interface, which is a serial communication controller coupled to the cabinet for data communication. Pet. 34; Ex. 1011, Figs. 2, 7, 8. Patent Owner argues that Petitioner does not explain how or why one of ordinary skill in the art would have combined the serial communication controller in Pocrass with Horst. Prelim. Resp. 34–36. Because Petitioner has shown sufficiently that Horst teaches a serial communication controller, for purposes of this decision, we do not rely on Petitioner's alleged rationale for combining the serial communication controller in Pocrass with Horst. On this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 56 would have been obvious over Horst, the LVDS Owner's Manual, and Pocrass.

Claim 59 depends from claim 54 and further recites that the computer module comprises "a connector distinct from the main circuit board, and the connector is configured to couple to the coupling site of the console for data communication." Ex. 1001, col. 43, l. 66–col. 44, l. 2. Petitioner argues that the processor node in Horst connects to the console through a backplane. Pet. 36; Ex. 1011, 1. Petitioner argues that Pocrass teaches a processor module that includes connectors distinct from a main circuit board that are configured to couple to the backplane of a chassis for data communication. Pet. 36; Ex. 1016, col. 16, ll. 9–15, Fig. 1. Petitioner argues that it would have been obvious to one of ordinary skill in the art to combine the connector in Pocrass with the processor node in Horst to allow for an easier connection with the backplane. Pet. 36; Ex. 1003 ¶¶ 136–138, 141–142.

Patent Owner argues that Petitioner does not explain how or why one of ordinary skill in the art would have combined the processor node in Horst

with the connector in Pocrass. Prelim. Resp. 36–37. Patent Owner's argument is not persuasive. As discussed above, Petitioner argues that Pocrass teaches a processor module that connects *to a console through a backplane*, similar to the processor module in Horst. Petitioner explains that, therefore, it would have been obvious to one of ordinary skill in the art to use the connector from Pocrass in a similar manner to connect the processor module in Horst *to a console through a backplane*. Pet. 36. On this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 59 would have been obvious over Horst, the LVDS Owner's Manual, and Pocrass.

5. *Obviousness of Claim 58 over Horst, LVDS Owner's Manual, and Deters*

Petitioner argues that claim 58 would have been obvious over Horst, the LVDS Owner's Manual, and Deters. Pet. 59–60. We have reviewed Petitioner's assertions and supporting evidence, and, for the reasons discussed below, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 58 would have been obvious over Horst, the LVDS Owner's Manual, and Deters.

Claim 58 depends from claim 54 and further recites that the computer module comprises "an enclosure housing the main circuit board, the processing unit, the main memory, the LVDS channel, and the interface controller, and the enclosure is insertable into the coupling site of the console." Ex. 1001, col. 43, ll. 61–65. Petitioner argues that Deters teaches using cartridges to enclose computer components and enable insertion into a modular computer chassis. Pet. 36–37; Ex. 1017, col. 3, ll. 3–7. Petitioner argues that it would have been obvious to one of ordinary skill in the art to enclose the processor node in Horst with the cartridge in Deters to prevent

damage to the computer components in the processor node. Pet. 37; Ex. 1003 ¶¶ 146–149. On this record, Petitioner demonstrates a reasonable likelihood of prevailing in showing that claim 58 would have been obvious over Horst, the LVDS Owner's Manual, and Deters.

6. *Obviousness of Claims 54, 57, 60, and 61 over Bogaerts and James or Gulick*

Petitioner argues that claims 54, 57, 60, and 61 would have been obvious over Bogaerts and James or Gulick. Pet. 59. Bogaerts relates to a scalable coherent interface for data acquisition. Ex. 1013, 1. We have reviewed Petitioner's assertions and supporting evidence, and, for the reasons discussed below, Petitioner does *not* demonstrate a reasonable likelihood of prevailing in showing that claims 54, 57, 60, and 61 would have been obvious over Bogaerts and James or Gulick.

Each independent claim challenged by Petitioner recites an encoded serial bit stream of Peripheral Component Interconnect (PCI) bus transaction. Ex. 1001, col. 43, ll. 48–49. Petitioner argues that Bogaerts teaches this limitation because the PCI-SCI adapter cards "allow 'transparent access of PCI memory space via SCI' and allow 'PCI Memory space [to be] transferred over distance via SCI.'" Pet. 42. Petitioner does not identify with specificity anything in Bogaerts that teaches or suggests that the aforementioned transfer of PCI memory space is *encoded*. *Id.* Further, the parts of Mr. Young's Declaration cited by Petitioner do not persuade us that Bogaerts teaches or suggests that the PCI memory transfer is encoded. Ex. 1003 ¶¶ 158, 159, 178[54D]. One paragraph of Mr. Young's Declaration, which was not cited by Petitioner, states that a person of ordinary skill in the art at the time "would also understand that, for the system to be able to interface with those peripheral components over a serial bus, the addressing

and data would need to be encoded." *Id.* ¶ 160. However, Mr. Young does not provide a sufficient explanation or credible evidence to support that conclusory statement. *Id.* Therefore, on this record, Petitioner does *not* demonstrate a reasonable likelihood of prevailing in showing that claims 54, 57, 60, and 61 would have been obvious over Bogaerts and James or Gulick.[4]

7. *Additional Grounds Based on Bogaerts*

Petitioner argues that claims 56 and 59 would have been obvious over Bogaerts, Pocrass, and James or Gulick, and that claim 58 would have been obvious over Bogaerts, Deters, and James or Gulick. Pet. 59. Petitioner also argues that claims 54 and 56–61 would have been obvious over any of the other grounds based on Bogaerts and further including the LVDS Owner's Manual. *Id.*at 60. Petitioner does not argue, however, that any of Pocrass, Deters, or the LVDS Owner's Manual teach or suggest the limitation discussed above in Section II.B.6 (i.e., an encoded serial bit stream of address and data bits of Peripheral Component Interconnect (PCI) bus transaction). Pet. 47–51. Therefore, for the same reasons discussed above in Section II.B.6, on this record, Petitioner does *not* demonstrate a reasonable likelihood of prevailing in showing that claims 54 and 56–61 would have been obvious over Bogaerts, Pocrass, Deters, the LVDS Owner's Manual, and James or Gulick.

III. CONCLUSION

Petitioner demonstrates a reasonable likelihood of prevailing on its challenge to the patentability of claims 54 and 56–61 of the '873 patent as

[4] Petitioner does not argue that it would have been obvious to combine an encoding feature from James or Gulick with Bogaerts. Pet. 41.

unpatentable under 35 U.S.C. § 103. At this stage in the proceeding, we have not made a final determination with respect to the patentability of any of the challenged claims.

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 54 and 56–61 of the '873 patent on the following grounds:

A. Claims 54, 57, 60, and 61 as unpatentable under 35 U.S.C. § 103(a) as obvious over Horst and the LVDS Owner's Manual;

B. Claims 56 and 59 as unpatentable under 35 U.S.C. § 103(a) as obvious over Horst, the LVDS Owner's Manual, and Pocrass; and

C. Claim 58 as unpatentable under 35 U.S.C. § 103(a) as obvious over Horst, the LVDS Owner's Manual, and Deters;

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '873 patent is hereby instituted commencing on the entry date of this Order, and, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; and

FURTHER ORDERED that the trial is limited to the grounds identified, and no other grounds are authorized.

Case IPR2014-01462
Patent 8,041,873 B2

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